Remarks

This Application has been carefully reviewed in light of the Office Action dated August 9, 2010. Applicants appreciate the Examiner's consideration of the Application. Although Applicants believe the claims are allowable without amendment, to advance prosecution Applicants have made clarifying amendments to Claims 1-12, 23, and 37. At least certain of these amendments are not considered narrowing, and none are considered necessary for patentability. Applicants respectfully request reconsideration and allowance of all pending claims.

I. The Claims Recite Statutory Subject Matter

The Examiner rejects Claims 1-11 and 37 under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Although Applicants believe these claims are directed to statutory subject matter without amendment, to advance prosecution Applicants have made clarifying amendments to these claims to obviate these rejections. As a point of clarification, Applicants assume the Examiner's mention of Claim 12 as being dependent on Claim 1 was a typographical error, and that the Examiner intended to list Claims 2-11 as being dependent on Claim 1. *See Office Action* at 2. For at least these reasons, Applicants respectfully request reconsideration and allowance of independent Claims 1 and 37 and their dependent claims.

II. Independent Claims 37-39 are Allowable

The Examiner rejects Claims 37-39 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Publication No. 2004/0103218 A1 by Blumrich, et al. ("*Blumrich*"), U.S. Patent 7,065,764 B1 to Prael, et al. (*"Prael"*), and Official Notice. Applicants respectfully traverse these rejections.

The proposed *Blumrich-Prael-Official Notice* combination fails to disclose, teach, or suggest at least the following limitations recited in Claim 37, which Applicants discuss as an example:

- each [of a plurality of nodes] comprising:
  at least two first processors integrated to a first card and operable to communicate with each other via a direct link between them; and
  a first switch integrated to the first card, the first processors communicably coupled to the first switch, the first switch operable to communicably couple the first processors to six or more second cards each

comprising at least two second processors integrated to the second card and a second switch integrated to the second card operable to communicably couple the second processors to the first card and at least five third cards each comprising at least two third processors integrated to the third card and a third switch integrated to the third card;

- the first processors being operable to communicate with particular second processors on a particular second card via the first switch and the second switch on the particular second card;
- the first processors being operable to communicate with particular third processors on a particular third card via the first switch, a particular second switch on a particular second card between the first card and the particular third card, and the third switch on the particular third card without communicating via either second processor on the particular second card.

For example, as allegedly disclosing that each node comprises "at least two first processors integrated to a first card and operable to communicate with each other via a direct link between them," the Examiner apparently relies on paragraph 57, lines 3-4 of *Blumrich*. *Office Action* at 11. The cited portion of *Blumrich* discloses that "[e]ach node contains a second processor for handling message passing operations." *Blumrich* at ¶0057. Even assuming that this portion discloses that a node may contain at least two processors, the cited portion does not disclose, teach, or suggest that the two processors are integrated to a first card, let alone that the two processors are operable to communicate with each other via a direct link between them (as would be necessary for the cited portion to even possibly disclose these claim limitations). Thus, the cited portion of *Blumrich* does not disclose, teach, or suggest "at least two first processors integrated to a first card and operable to communicate with each other via a direct link between them," as recited in Claim 37.

As another example, as allegedly disclosing "the first processors communicably coupled to the first switch, the first switch operable to communicably couple the first processors to six or more second cards each comprising at least two second processors integrated to the second card and a second switch integrated to the second card operable to communicably couple the second processors to the first card and at least five third cards each comprising at least two third processors integrated to the third card and a third switch integrated to the third card," the Examiner apparently relies on paragraph 203, lines 8-10 and Figures 1 and 5 of *Blumrich*. Paragraph 203 of *Blumrich* discloses that the "minimum partition consists of an 8x8x8 Torus plus 8 I/O Nodes, and partitions can increase in any

dimension in multiples of 8 nodes." In other words, the cited portion at best discloses that *Blumrich* contemplates multidimensional nodes. It is not entirely clear on which portions of Figures 1 and 5 the Examiner relies as allegedly disclosing these limitations. Figure 1 generally shows a three-dimensional Torus interconnecting eight computing nodes. *See Blumrich* at Figure 1 and ¶0035. Figure 5 generally shows a global combining tree network including global signals and external network connections. *See Blumrich* at Figure 5 and ¶0039. In other words, it again appears to Applicants that the cited portion discloses that *Blumrich* contemplates multidimensional nodes. However, merely disclosing multidimensional nodes does not disclose the numerous above-listed particular limitations explicitly recited in this portion of Claim 37.

To elaborate, merely disclosing multidimensional nodes does not disclose that each node comprises "[at least two] first processors [integrated to a first card] communicably coupled to the first switch [integrated to the first card]," as recited in Claim 37. Additionally, merely disclosing multi-dimensional nodes does not disclose that a first switch [integrated to the card] that is operable to communicably couple the first processors to six or more second cards each comprising at least two second processors integrated to the second card and a second switch integrated to the second card operable to communicably couple the second processors to the first card and at least five third cards each comprising at least two third processors integrated to the third card and a third switch integrated to the third card, as recited in Claim 37.

Furthermore, the Examiner apparently acknowledges that *Blumrich* does not disclose "**a first switch integrated to the first card.**" *Office Action* at 12. Thus, it is unclear how the cited portion of *Blumrich* could possibly disclose, as alleged by the Examiner, "the first processors communicably **coupled to the first switch, the first switch operable to** communicably couple the first processors to **six or more second cards each comprising** at least two second processors integrated to the second card and **a second switch integrated to the second card** operable to communicably couple the second processors to the first card and **at least five third cards each comprising** at least two third processors integrated to the third card and **a third switch integrated to the third card**," as recited in Claim 37.

As another example, the cited portions of *Blumrich* fail to disclose, teach, or suggest "the first processors being operable to communicate with particular second processors on a particular second card via the first switch and the second switch on the particular second card," as recited in Claim 37. As allegedly disclosing these limitations, the Examiner cites paragraph 57, lines 1-14 of *Blumrich*. The cited portion of *Blumrich* discloses the following:

> In the described embodiment, system packaging comprises 512 processing nodes on a doubled-sided board or "midplane". Each node contains a second processor for handling message passing operations. In addition, associated with a prescribed plurality of processing nodes is a dedicated I/O node that comprises a dual-processor with expanded external memory, for handling of I/O communications to and from the compute nodes. Each I/O node has a small operating system that can handle basic I/O tasks and all the functions necessary for high performance real time code. For compiling, diagnostics, and analysis a host machine is required. The I/O nodes contain a software layer above the layer on the compute nodes for handling host communications.

Blumrich at ¶0057, lines 1-14. While the cited portion discloses that one of the plurality of processing nodes is a dedicated I/O node, which Applicants assume the Examiner is attempting to equate to the claimed first switch (or at least to the component operable to perform the operations of the claimed first switch), the cited portions do not disclose that, for each node, the processors of the node are operable to communicate via a switch integrated to a card of the node to particular second processors on a particular second card in a second switch integrated to the second card, as recited in Claim 37. In fact, given that the Examiner appears to apply the nodes of *Blumrich* to the claimed nodes, it is unclear how *Blumrich*'s disclosure of a separate node as a dedicated I/O node could possibly disclose that each node comprises a first switch and that "the first processors [of the node are] operable to communicate with particular second processors on a particular second card via the first switch and the second switch on the particular second card," as recited in Claim 37.

As yet another example, Applicants respectfully traverse the Official Notice taken by the Examiner with respect to, in the Examiner's words, "two processors on a card that communicate with a central authority without communicating via either second processor on the particular second card." *Office Action* at 12.

First, the limitations to which Applicants assume the Examiner is referring actually recite that "the first processors [is] operable to communicate with particular third processors

on a particular third card via the first switch, a particular second switch on a particular second card between the first card and the particular third card, and the third switch on the particular third card without communicating via either second processor on the particular second card."

Second, while in limited circumstances an examiner may take official notice of facts not in the record or rely on "common knowledge" in making a rejection, "such rejections should be judiciously applied." *See* M.P.E.P. § 2144.03. It is not appropriate for an examiner to take official notice of facts without citing a prior art reference "where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known. For example, assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must always be supported by citation to some reference work recognized as standard in the pertinent art." *Id.* (citing *In re Ahlert*, 165 U.S.P.Q. 418, 420-21 (C.C.P.A. 1970)). To the extent that the Examiner maintains this rejection based on "Official Notice," "well-known art," "common knowledge," or other information within the Examiner's personal knowledge, Applicants respectfully request that the Examiner cite a reference as documentary evidence in support of this position or provide an affidavit in accordance with M.P.E.P. § 2144.03 and 37 C.F.R. § 1.107.

Specifically, the Examiner states, "the purpose of multi-processing is to improve the efficiency of processing tasks and therefore, not having the two processors communicate would require a third authority to designate the tasks, just increasing overhead of the system and therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to modify the teachings of the combination of *Blumrich* and *Fung* to utilize processors that don't co-communicate." *See Office Action* at 12-13. Applicants do not necessarily agree. For example, "increasing overhead of the system" may provide a reason that a person of ordinary skill in the art would **not** include a central authority, and would instead use processors that communicate via either second processor on the particular second card.[1] As another example, it is not necessarily technically possible that one of ordinary skill

[1] In response to this argument, the Examiner states that "the argument the Examiner intended to make was that the technology was well known, but that it would have likely made the system less efficient; thus, they decided not to implement the technology." *Office Action* at 15. Respectfully, this speculative argument does not seem to bolster the Examiner's position that the claim limitations were supposedly well known in the art. Instead, the Examiner's clarification again highlights that the Examiner is merely assuming - without any support - that the "the technology was well known," and then further assumes that one of ordinary skill in the art would have disregarded that supposedly well-known approach.

in the art at the time of Applicants' invention could have simply modified existing systems in the manner suggested by the Examiner. Despite Applicants' requests, it does not appear to Applicants that the Examiner has provided a reference in support of the Examiner's position for this taking of Official Notice. *See* M.P.E.P. § 2144.03.

Independent Claim 38 recites that each of a plurality of nodes comprises at least two first processors and a first switch. The at least two first processors are integrated to a first card and operable to communicate with each other via a direct link between them. The first switch is integrated to the first card. The first processors are communicably coupled to the first switch, and the first switch is operable to communicably couple the first processors to six or more second cards each comprising at least two second processors integrated to the second card and a second switch integrated to the second card operable to communicably couple the second processors to the first card and at least five third cards each comprising at least two third processors integrated to the third card and a third switch integrated to the third card. The first processors are operable to communicate with particular second processors on a particular second card via the first switch and the second switch on the particular second card. The first processors are operable to communicate with particular third processors on a particular third card via the first switch, a particular second switch on a particular second card between the first card and the particular third card, and the third switch on the particular third card without communicating via either second processor on the particular second card. Applicants respectfully submit that, for at least certain reasons analogous to those discussed above with respect to Claim 37, the proposed *Blumrich-Prael-Official Notice* combination fails to disclose, teach, or suggest these limitations of Claim 38.

Independent Claim 39 recites that each of a plurality of nodes comprises at least two first processors and a first switch. The at least two first processors are integrated to a first card and operable to communicate with each other via a direct link between them. The first switch is integrated to the first card. The first processors are communicably coupled to the first switch, and the first switch is operable to communicably couple the first processors to six or more second cards each comprising at least two second processors integrated to the second card and a second switch integrated to the second card operable to communicably couple the second processors to the first card and at least five third cards each comprising at least two

third processors integrated to the third card and a third switch integrated to the third card. The first processors are operable to communicate with particular second processors on a particular second card via the first switch and the second switch on the particular second card. The first processors are operable to communicate with particular third processors on a particular third card via the first switch, a particular second switch on a particular second card between the first card and the particular third card, and the third switch on the particular third card without communicating via either second processor on the particular second card. Applicants respectfully submit that, for at least certain reasons analogous to those discussed above with respect to Claim 37, the proposed *Blumrich-Prael-Official Notice* combination fails to disclose, teach, or suggest these limitations of Claim 39.

Additionally, Applicants do not admit that the proposed combination and modifications of these references are possible or that the Examiner has provided an adequate reason to combine or modify the references in the manner proposed. In light of the numerous deficiencies discussed above and to avoid burdening the record, Applicants do not discuss the impropriety of the proposed combination and modifications in this Response. However, Applicants reserve the right to discuss the impropriety in a future Response or on Appeal if appropriate.

For at least these reasons, Applicants respectfully request reconsideration and allowance of independent Claims 37-39.

III. Independent Claims 1, 12, and 23 and their Dependent Claims are Allowable over the Proposed *Blumrich-Prael* Combination

The Examiner rejects Claims 1-3, 9, 12-14, 23-25, and 34-36 under 35 U.S.C. § 103(a) as being unpatentable over the proposed *Blumrich-Prael* combination. Applicants traverse the rejections and discuss independent Claim 1 as an example.

The rejection of Claim 1 is improper at least because the proposed *Blumrich-Prael* combination fails to disclose, teach, or suggest each element of Claim 1. For example, the proposed *Blumrich-Prael* combination fails to disclose, teach, or suggest at least the following limitations recited in amended Claim 1:

- a plurality of cluster agents, each cluster agent associated with one of a plurality of nodes, each node comprising a switching fabric integrated to a card and **at least two processors integrated to the card, the at least two processors operable to communicate with each other via a direct link between them and communicably coupled to the switching fabric integrated to the card, the switching fabric operable to communicably couple, via another switch integrated to another card of another node, the at least two processors to at least two processors integrated to the other card of the other node**.

In response to Applicants' previous argument that the proposed *Blumrich-Prael* combination fails to disclose "a plurality of nodes, **each node comprising a switching fabric integrated to a card**" as recited in Claim 1 (even prior to the amendments presented in this Response), and that the Examiner has provided no evidence that the claimed "switching fabric" is indeed necessary for the communication between multiple processors on a single board of a symmetric multiprocessor, as alleged by the Examiner, the Examiner cited U.S. Patent 6,633,945 to Fu, at al. ("*Fu*") as allegedly disclosing that "multiprocessors contain a switching fabric between them." *See Office Action* at 13-14. Even assuming for the sake of argument only and without concession that *Fu* discloses that "multiprocessors contain a switching fabric between them," as alleged by the Examiner, the cited portions of the proposed *Blumrich-Prael* combination would still fail to disclose the above-identified limitations of amended Claim 1.

For example, as discussed above with respect to Claim 37, the cited portion of *Blumrich* fails to disclose, teach, or suggest "at least two processors [integrated to a card of the node] operable to communicate with each other via a direct link between them. The Examiner does not appear to allege that *Prael* makes up for this deficiency of *Blumrich*.

As another example, neither *Blumrich* nor *Prael* appears to disclose that the at least two processors are "communicably coupled to the switching fabric integrated to the card," and that "the switching fabric [is] operable to communicably couple, via another switch integrated to another card of another node, the at least two processors to at least two processors integrated to the other card of the other node," as recited in Claim 1 as amended.

The cited portion of *Fu* does not appear to make up for this deficiency of *Blumrich* and *Prael*, and the Examiner does not appear to make any assertion that it does.

Independent Claim 12 recites a method that includes determining a status of each of at least a subset of a plurality of nodes. Each node comprises a switching fabric integrated to a card and at least two processors integrated to the card. The at least two processors are operable to communicate with each other via a direct link between them, and are communicably coupled to the switching fabric integrated to the card. The switching fabric is operable to communicably couple, via another switch integrated to another card of another node, the at least two processors to at least two processors integrated to the other card of the other node. Applicants respectfully submit that, for at least certain reasons analogous to those discussed above with respect to Claim 1, the proposed *Blumrich-Prael* combination fails to disclose, teach, or suggest these limitations of Claim 12.

Independent Claim 23 recites a system that includes a plurality of computing nodes, each computing node comprising a switching fabric integrated to a card and at least two processors integrated to the card. The at least two processors are operable to communicate with each other via a direct link between them, and are communicably coupled to the switching fabric integrated to the card. The switching fabric is operable to communicably couple, via another switch integrated to another card of another computing node, the at least two processors to at least two processors integrated to the other card of the other computing node. Applicants respectfully submit that, for at least certain reasons analogous to those discussed above with respect to Claim 1, the proposed *Blumrich-Prael* combination fails to disclose, teach, or suggest these limitations of Claim 23.

Additionally, Applicants do not admit that the proposed combination and modifications of these references are possible or that the Examiner has provided an adequate reason to combine or modify the references in the manner proposed. In light of the numerous deficiencies discussed above and to avoid burdening the record, Applicants do not discuss the impropriety of the proposed combination and modifications in this Response. However, Applicants reserve the right to discuss the impropriety in a future Response or on Appeal if appropriate.

For at least these reasons, Applicants respectfully request reconsideration and allowance of independent Claims 1, 12, and 23 and their dependent claims.

IV. The Separately-Rejected Dependent Claims are Allowable

The Examiner rejects Claims 4-5, 8, 10-11, 15-16, 19-22, 26-27, and 30-33 under 35 U.S.C. § 103(a) as being unpatentable over *Blumrich* in view of *Prael* and further in view of "The Cactus Worm: Experiments with Dynamic Resource Discovery and Allocation in a Grid Environment" by Allen, et al. ("*Allen*"). The Examiner rejects Claims 6-7, 17-18, and 28-29 under 35 U.S.C. § 103(a) as being unpatentable over *Blumrich* in view of *Prael* and *Allen*, and further in view of U.S. Publication No. 2003/0217105 A1 by Zircher, et al. ("*Zircher*"). Applicants respectfully traverse these rejections.

Claims 4-8, 10-11, 15-22, 26-33 depend from independent claims shown above to be allowable. The Examiner has not alleged that the cited portions of *Allen* and *Zircher* cure the deficiencies of *Blumrich* and *Prael* discussed above with respect to Claim 1. Thus, dependent Claims 4-8, 10-11, 15-22, 26-33 are allowable at least because they depend from allowable independent claims. In addition, dependent Claims 4-8, 10-11, 15-22, 26-33 recite further patentable distinctions over the proposed combinations. To avoid burdening the record and in view of the clear allowability of independent Claims 1, 12, and 23, Applicants do not discuss in this Response the further patentable distinctions recited in these claims. However, Applicants reserve the right to discuss these distinctions in a future Response or on Appeal, if appropriate. Furthermore, Applicants do not admit that the proposed combinations of references are possible or that the Examiner has provided an adequate explanation for combining or modifying the references in the manner proposed.

For at least these reasons, Applicants respectfully request reconsideration and allowance of Claims 4-8, 10-11, 15-22, and 26-33.

V. Request for Evidentiary Support

Should a rejection based on any of the above asserted rejections be maintained, Applicants respectfully request appropriate evidentiary support. Additionally, if the Examiner is relying upon "common knowledge" or "well known " principles to establish the rejection, Applicants request that a reference be provided in support of this position pursuant

to M.P.E.P. § 2144.03. Furthermore, to the extent that the Examiner maintains any rejection based on an "Official Notice" or other information within the Examiner's personal knowledge, Applicants respectfully request that the Examiner cite a reference as documentary evidence in support of this position or provide an affidavit in accordance with M.P.E.P. § 2144.03 and 37 C.F.R. 1.104(d)(2).

VI. No Waiver

All of Applicants' arguments and amendments are without prejudice or disclaimer. Additionally, Applicants have merely discussed example distinctions from the references cited by the Examiner. Other distinctions may exist, and Applicants reserve the right to discuss these additional distinctions in a later Response or on Appeal, if appropriate. By not responding to additional statements made by the Examiner, Applicants do not acquiesce to the Examiner's additional statements. The example distinctions discussed by Applicants are sufficient to overcome the Examiner's rejections.

Conclusion

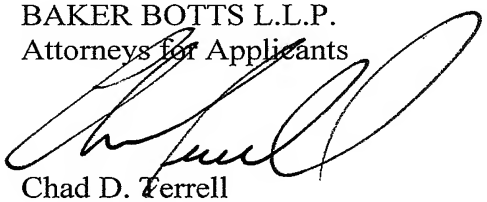
Applicants have made an earnest attempt to place this Application in condition for allowance. For at least the foregoing reasons, Applicants respectfully request full allowance of all pending claims.

If the Examiner feels that a telephone conference would advance prosecution of this Application in any manner, the Examiner is invited to contact Chad D. Terrell, Attorney for Applicants, at (214) 953-6813 at the Examiner's convenience.

The Commissioner is hereby authorized to charge the amount of $130.00 to Deposit Account No. 02-0384 of Baker Botts L.L.P. for a one-month extension of time. Although Applicants believe that no other fees are due, the Commissioner is hereby authorized to charge any other necessary fees and credit any overpayments to Deposit Account No. 02-0384 of Baker Botts L.L.P.

Respectfully submitted,

BAKER BOTTS L.L.P.
Attorneys for Applicants



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Date: December 9, 2010

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